CLAIMS

1. A method of manufacturing a semiconductor device, comprising the steps of:

a) forming, on one major surface of a substrate,

a gate structure constituted by either one of a dummy gate electrode and a gate electrode having an insulating film at least on bottom surface, and

a device isolation insulating film

so as to form a first groove divided by said dummy gate electrode or said gate electrode, to position said dummy gate electrode or said gate electrode in the first groove, and to form said gate structure to have an upper surface level not higher than an upper level of said device isolation insulating film; and

b) forming source and drain electrodes in the first groove.

2. A method according to claim 1, wherein

said gate structure is one selected from the group consisting of

a first gate structure consisting of a dummy gate wiring layer and said dummy gate electrode, and

a second gate structure consisting of a gate wiring layer having a insulating film at least on bottom surface and said gate electrode,

said dummy gate wiring layer or said gate wiring layer is formed on the device isolation insulating film, connected to said dummy gate electrode or said gate

electrode, and crossing said first groove.

3. A method according to claim 1, further comprising the step of respectively forming a source diffusion layer and drain diffusion layer in a surface region of said substrate corresponding to the first groove before the step of forming said source and drain electrodes.

4. A method according to claim 1, further comprising:

the steps of, before the step of forming said source and drain electrode, forming a semiconductor film using epitaxial growth on a bottom surface of the first groove; and

respectively forming source and drain diffusion layers in said semiconductor film.

5. A method according to claim 1, wherein the step of forming said source and drain electrodes comprises:

forming, on one entire major surface of said substrate, a first thin film made of either one of a material constituting said source and drain electrodes and a material used to form said source and drain electrodes; and

removing a portion of said first thin film located outside the first groove by using CMP.

6. A method according to claim 2, wherein said gate structure is the first gate structure, and

the method further comprises the steps of:

removing said first gate structure to form a second groove after the step of forming said source and drain electrodes; and

forming an insulating film, a gate electrode, and a gate wiring layer in the second groove so that said gate electrode divides the gate wiring layer and positions between said source electrode and said drain electrode, and so that said insulating film is interposed between said gate wiring layer and an inner wall of the second groove.

7. A method according to claim 6, wherein said gate electrode and said gate wiring layer are simultaneously formed in one piece by:

forming a second thin film made of either one of a material constituting said gate wiring layer and material used to form said gate wiring layer, on one entire major surface of said substrate; and

removing a portion of said second thin film located outside the second groove by using CMP.

8. A method according to claim 2, wherein the step of forming said gate structure and said device isolation insulating film comprises:

forming said device isolation insulating film on one major surface of said substrate;

forming a third groove in said device isolation insulating film;

forming, on one entire major surface of said substrate, a third thin film made of a material constituting said gate structure;

removing a portion of said third thin film located outside the third groove by using CMP; and

forming the first groove, at least a part of the sidewall of which is constituted by said device isolation insulating film, so as to cross the gate structure.

9. A method according to claim 1, wherein said source and drain electrodes are made of a metal.

10. A method according to claim 1, wherein said gate structure is the second gate structure, and said gate electrode and said gate wiring layer are made of a metal.

11. A method according to claim 1, wherein said gate structure is one selected from the group consisting of said dummy gate electrode and said gate electrode having the insulating film at least on bottom surface.

12. A method according to claim 11, wherein the step of forming said gate structure and said device isolation insulating film comprises forming a dummy wiring layer which is positioned above part of said device isolation insulating film, and said gate structure, and has an upper surface level higher than the upper surface level of said device isolation

insulating film.

13. A method according to claim 12, further comprising the steps of, before the step of forming said source and drain electrodes:

forming a fourth thin film on one entire major surface of said substrate;

polishing said fourth thin film and exposing an upper surface of said dummy wiring layer; and

removing said dummy wiring layer to form a fourth groove in said forth thin film.

14. A method according to claim 13, further comprises the step of removing at least a part of an exposed portion of said device isolation insulating film in the fourth groove to form a eighth groove in a bottom of said fourth groove, between the step of forming the fourth groove and the step of forming said source and drain electrodes.

15. A method according to claim 13, wherein said gate structure is the dummy gate electrode, and

the method further comprises the steps of, between the step of forming said fourth groove and the step of forming said source and drain electrodes,

removing said dummy gate electrode to form a seventh groove in a bottom of said fourth groove; and

forming a gate electrode in the fourth groove.

16. A method according to claim 13, wherein said fourth thin film is made of either one of a material

constituting said source and drain electrodes and material used to form said source and drain electrodes.

17. A method according to claim 13, further comprising the step of removing said fourth thin film before the step of forming said source and drain electrodes.

18. A method according to claim 13, further comprising the steps of, after the step of forming said device isolation insulating film and said gate structure:

removing a portion of said device isolation insulating film to form a fifth groove; and

forming, in the fifth groove, a connection wiring layer connected to at least one of said source electrode, said drain electrode, and said gate wiring layer.

19. A method according to claim 18, wherein the step of forming said connection wiring layer and the step of forming said source and drain electrodes are performed simultaneously.

20. A method according to claim 15, further comprising the steps of, after the step of forming said device isolation insulating film and said gate structure:

removing a portion of said device isolation insulating film to form a fifth groove; and

forming, in the fifth groove, a connection wiring

layer connected to at least one of said source electrode, said drain electrode, and said gate wiring layer,

wherein the step of forming said gate wiring layer and the step of forming said connection wiring layer are performed simultaneously.

21. A method according to claim 1, wherein the step of forming said gate structure and said device isolation insulating film comprises:

forming, on one entire major surface of said substrate, a third thin film made of a material constituting said dummy gate wiring layer;

forming a sixth forward-tapered groove in said third thin film;

forming said device isolation insulating film on one major surface of said substrate;

removing a portion of said device isolation insulating film located outside the sixth groove by using CMP; and

anisotropically etching said third thin film to simultaneously form said gate structure and first groove, and a sidewall on a side surface of said device isolation insulating film.

22. A method according to claim 6, further comprising the steps of, before the step of forming said insulating film and said gate wiring layer:

doping; with a conductive impurity, a surface

region of said substrate corresponding to the second groove; and

forming a semiconductor film on a bottom surface of the second groove by using epitaxial growth.

23. A method of manufacturing a semiconductor device, comprising the steps of:

forming a dummy gate wiring layer on one major surface of a substrate;

forming a semiconductor film on an exposed surface of one major surface of a substrate;

forming a semiconductor film on an exposed surface of one major surface of said substrate by using epitaxial growth; and

forming, on said semiconductor film, a gate sidewall which is made of an insulator and covers a side surface of said dummy gate wiring layer.

24. A method according to claim 23, further comprising the steps of, after the step of forming said gate sidewall:

forming an interlayer insulating film on one entire major surface of said substrate;

flattening said interlayer insulating film so as to expose an upper surface of said dummy gate wiring layer;

removing said dummy gate wiring layer to form a groove;

forming an gate insulating film on a bottom

surface and a sidewall of the groove; and

forming a gate wiring layer in the groove.

25. A method according to claim 24, further comprising the step of doping said semiconductor film with a conductive impurity before the step of forming said gate sidewall.

26. A method according to claim 25, further comprising the step of doping a surface region of one major surface of said substrate and said semiconductor film with a conductive impurity between the step of forming said gate sidewall and step of forming said interlayer insulating film.

27. A method according to claim 24, wherein the step of forming said semiconductor film comprises epitaxially growing a semiconductor containing a conductive impurity.

28. A method according to claim 27, further comprising the step of doping a surface region of one major surface of said substrate and said semiconductor film with a conductive impurity between the step of forming said gate sidewall and step of forming said interlayer insulating film.

29. A method according to claim 24, wherein the step of forming said gate wiring layer comprises:

depositing either one of a conductor and a semiconductor material on one major surface of said substrate so as to fill the groove; and

removing a portion of said conductor or semiconductor material located outside the groove.

30. A semiconductor device comprising:

a substrate;

a device isolation insulating film formed on one major surface of said substrate,

a gate electrode formed on one major surface of said substrate;

a gate wiring layer formed on said device isolation insulating film and connected to said gate electrode;

a source electrode and drain electrode arranged on one major surface of said substrate to face each other via said gate electrode; and

an insulating film formed on a bottom surface and a side surface of said gate electrode and said gate wiring layer; and

wherein said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film.

31. A device according to claim 30, further comprising a source diffusion layer and a drain diffusion layer below said source electrode and said drain electrode of said substrate.

32. A device according to claim 31, wherein said

gate electrode and said gate wiring layer have bottom surfaces lower than upper surfaces of said source and drain diffusion layers.

33. A device according to claim 30, wherein said gate electrode, said gate wiring layer, and said source and drain electrodes have upper surface levels equal to each other.

34. A device according to claim 30, wherein said gate electrode and said gate wiring layer have upper surface levels lower than upper surface levels of said source and drain electrodes.

35. A device according to claim 30, wherein said gate electrode and said gate wiring layer have upper surface levels higher than upper surface levels of said source and drain electrodes.

36. A device according to claim 30, further comprising a connection wiring layer connected to at least one of said source electrode, said drain electrode, said gate electrode, and said gate wiring layer on one major surface of said substrate,

said connection wiring layer having an upper surface level equal to or lower than the upper surface level of said device isolation insulating film.

37. A semiconductor device comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film formed between said substrate and said gate wiring layer and on a side surface of said gate wiring layer;

a pair of thin films formed by epitaxial growing a semiconductor on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator.

38. A device according to claim 37, wherein a region of said pair of thin films between said gate sidewall and said substrate, a remaining region of said pair of thin films, and a surface region of said substrate in contact with the remaining region contain a conductive impurity.